In the Specification:

Please replace the paragraph beginning at page 7, line 22, with the following paragraph:

Referring now to Figure 2, there is shown a circuit diagram of exemplary sensing circuit 200 according to one embodiment of the present invention. Sensing circuit 200 can be part of a larger circuit arrangement (not shown) which itself may be part of a memory device. For example, sensing circuit 200 may be used for multi-level charge ("MLC") flash memory devices. To ~~illustrates~~ illustrate the features of the invention, reference will be made to exemplary memory cells capable of storing four different charge levels, wherein the current drawn by the memory cell corresponds to the charge level stored by the memory cell, where, for example, a first charge level corresponds to "00," a second charge level corresponds to "01," a third charge level corresponds to "10" and a fourth charge level corresponds to "11." In one particular embodiment, the first charge level draws approximately 0 microamperes (μA), the second charge level draws approximately 10 μA, the third charge level draws approximately 15 μA, and the fourth charge level draws 20 approximately μA. As discussed below, due to the particular arrangement of sensing circuit 200, sensing circuit 200 achieves efficient and accurate memory cell sensing for low voltage flash memory device.

PAGE 8/22 * RCVD AT 10/28/2004 8:45:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:9492821002 * DURATION (mm-ss):05-00

Please replace the paragraph beginning at page 9, line 3, with the following paragraph:

Also shown in Figure 2, the gate of transistor 234 is coupled to the gate of transistor 232, the source of transistor 234 is coupled to VCC 208, and the drain of transistor 234 is connected to node 242. Node 242 is connected to ground 210 through resistive load [[234]] 238, which may, for example, be a bias transistor.